JiaYu Zhao

Electronic Information Engineering | FPGA, Embedded Systems and Communications

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EDUCATION

UNIVERSITY
Harbin University of Science and Technology

DEGREE
B.Eng. in Electronic Information Engineering

DATES
2021 - 2025

COURSEWORK
Signals and Systems, Digital Circuits, Analog Electronics, C Programming, Microcontrollers

CAREER FOCUS

FPGA and embedded systems, electronic hardware development, communications and DSP roles.

AWARDS AND CREDENTIALS

University Scholarship
Awarded during undergraduate study.

Second Prize in Mathematical Modeling
Accurate localization of multiple rocket debris objects.

CET-4
Technical reading and English knowledge-base practice.

LEADERSHIP

Youth Volunteer Association | Team Captain
2022.01 - 2023.12

Coordinated event support, marathon operations and elder-care volunteering; developed task ownership and teamwork.

TECHNICAL STACK

FPGA: Verilog, Quartus, ModelSim, TimeQuest, DDS, QPSK, UART, I2C

Embedded: C, STM32 HAL, FreeRTOS, PWM, ADC, DMA, encoders, PID, Flash

DSP: MATLAB, BER, FFT, sampling, spectra, filtering, features

Circuits: Altium Designer, Multisim, PCB design and soldering, Keil

Software: Python, OpenCV, NumPy, data structures, Git, Linux, Docker, SQLite/MySQL, CMake, documentation

STRENGTHS

- Connect theory, implementation and verification in engineering work.
- Develop and debug in Windows and Linux environments.
- Document technical work and share reusable knowledge.
- Interested in photography and knowledge sharing.

PUBLIC CONTACT

No phone number, age, gender, salary expectation, preferred city or previous email is included in this public version.

PROFILE

Electronic information engineering graduate building practical workflows across communications, DSP, FPGA RTL, STM32/FreeRTOS and Python. Projects retain source, tests, constraints, build evidence, scripts, documentation and known limits.

- Break systems into independently verifiable algorithm, timing, interface and presentation layers.
- Debug from waveforms, logs, serial data, scripts and build reports.
- Separate simulation, compilation, timing closure and physical verification claims.

SELECTED PROJECTS

FPGA QPSK Baseband Link and Visualization

Verilog | UART | Python | Cyclone IV E

PRBS7, Gray mapping, discrete phase channel, hard decisions, BER counting and UART/CSV telemetry with Python constellation and I/Q views.

- Resolved pipeline alignment, signed widths and UART throughput limits.
- ModelSim and CSV paths pass; Quartus timing checks produce a .sof image.

Compilation and simulation complete; physical UART confirmation pending.

Multi-Function FPGA DDS Signal and Measurement System

DDS | I2C | PCF8591 AD/DA | 74HC595

Four-waveform DDS, ADC/DAC access, sample statistics and a six-digit display in one synthesizable Cyclone IV E design.

- Implemented a 32-bit phase accumulator, 256-entry LUT, I2C state machine and exponential average.
- ModelSim passes; Quartus synthesis, fitting, assembly and TimeQuest complete.

Compilation and simulation complete; analog board measurement pending.

STM32F103 FreeRTOS Multi-Mode Smart Car

C | FreeRTOS | PID | Encoders | C8T6/RCT6

Dual-wheel PID, odometry, line following, avoidance, Flash parameters, safety protection and Bluetooth command firmware.

- Seven task areas around a 10 ms control loop with diagnostics and watchdog protection.
- Both targets cross-build; PID and protocol host tests pass; ELF/HEX/BIN/MAP artifacts produced.

Software build complete; vehicle electrical, mechanical and calibration tests pending.

Mathematical Modeling: Accurate Localization of Multiple Rocket Debris Objects

Mathematical Modeling | Localization Analysis | Second Prize

Modeled and analyzed the accurate localization of multiple rocket debris objects.

- Translated the real-world positioning problem into solvable constraints and completed the competition submission.

Competition project; Second Prize in Mathematical Modeling.

STM32F103 Dual-Channel Temperature Monitoring and Alarm System

STM32 | DS18B20 | PT100 | OLED | FatFs

Samples a DS18B20 and PT100 module voltage, with OLED display, threshold alarms, SD CSV logging, serial configuration and persistent Flash thresholds.

- Non-blocking periodic scheduling coordinates acquisition, alarms, display, storage and serial tasks.
- Includes HAL, Keil/CubeMX, FatFs, documentation and a flashable HEX; ESP-01S cloud flow is disabled by default.

Independent development | 2024.05 - 2024.06 | Public repository packaged 2026.07

STM32 Vision-Guided Robotic Arm Sorter

STM32 | FreeRTOS | OpenCV | Inverse Kinematics

Vision-guided sorting with color detection, four-point calibration, CRC16 UART, inverse kinematics and FSR grasp confirmation.

- Simulator, 14 automated tests and GUI smoke test pass; firmware cross-build produces ELF/HEX/BIN/MAP.
- Five PWM channels, four RTOS tasks, workspace checks, smooth motion, E-stop and retry handling.

Team member 2023.05 - 2023.06 | Public repository packaged 2026.07 | Hardware validation pending

ENGINEERING METHOD

- Define acceptance criteria before implementation.
- Verify modules independently with waveforms, logs, scripts and build reports.
- Package source, constraints, results and known limits for reproducible handoff.